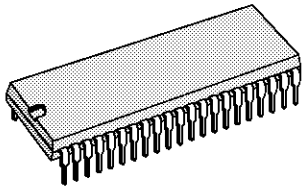
SGS-THOMSON MICROELECTRONICS

STV3951

MULTI PICTURE-IN-PICTURE PROCESSOR

ADVANCE DATA

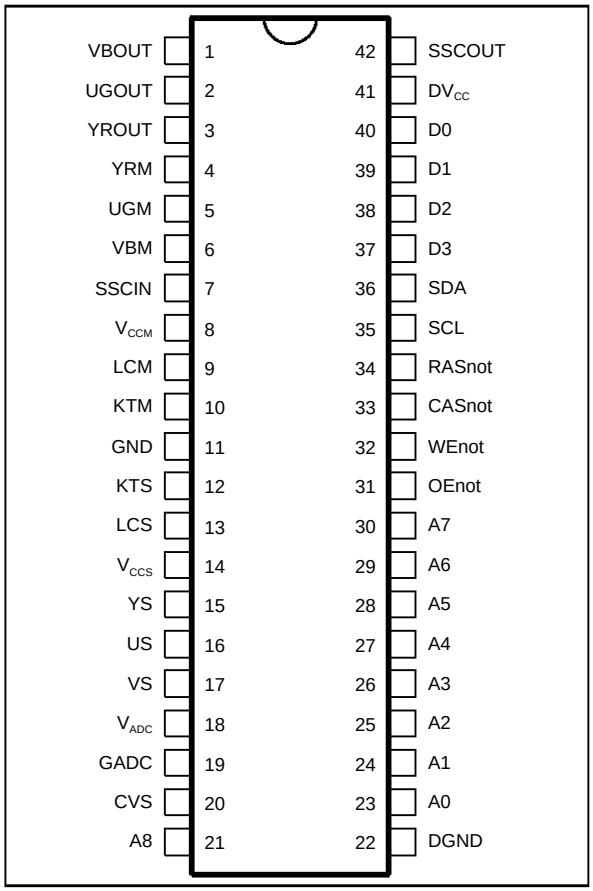
- Y, R-Y, B-Y INPUTS FOR SMALL PICTURE
- INTEGRATED ANTI ALIASING LOW-PASS FILTERS
- VERTICAL FILTERING ON CHROMA AND LUMINANCE
- 6 BITS PRECISE CONVERSION ON Y, R-Y AND B-Y
- FORMAT REDUCTION BY 3 OR 4
- DISPLAY OF 1 TO 4 SMALL PICTURES
- PROGRAMMATION OF :
  - BORDER COLOR (8 COLORS)
  - VERTICAL AND HORIZONTAL POSITION
  - SMALL PICTURE LUMINANCE GAIN
  - CONTRAST AND SATURATION OF SMALL PICTURES
- I^2C BUS CONTROLLED
- INTERNAL SWITCH FOR INSERTION INTO MAIN PICTURE
- Y, R-Y, B-Y OR R, G, B FORMAT OF MAIN PICTURE AND OUTPUTS
- POSSIBILITY TO USE AN EXTERNAL SWITCH
- 50Hz AND 60Hz MODES WITH AUTOMATIC RECOGNITION
- ADJUSTMENT FREE FOR MANUFACTURING
- SHRINK42 PACKAGE



SHRINK 42
(Plastic Package)

ORDER CODE : STV3951

PIN CONNECTIONS



3951-01.EPS

DESCRIPTION

The PIP processor provides all the functions necessary to process the size reduction of a 4/3 TV picture in the format Y, R-Y, B-Y, and to allow a very low cost multi-PIP application with only a chroma decoder, a standard DRAM, and a very few external components.

PIN CONNECTIONS

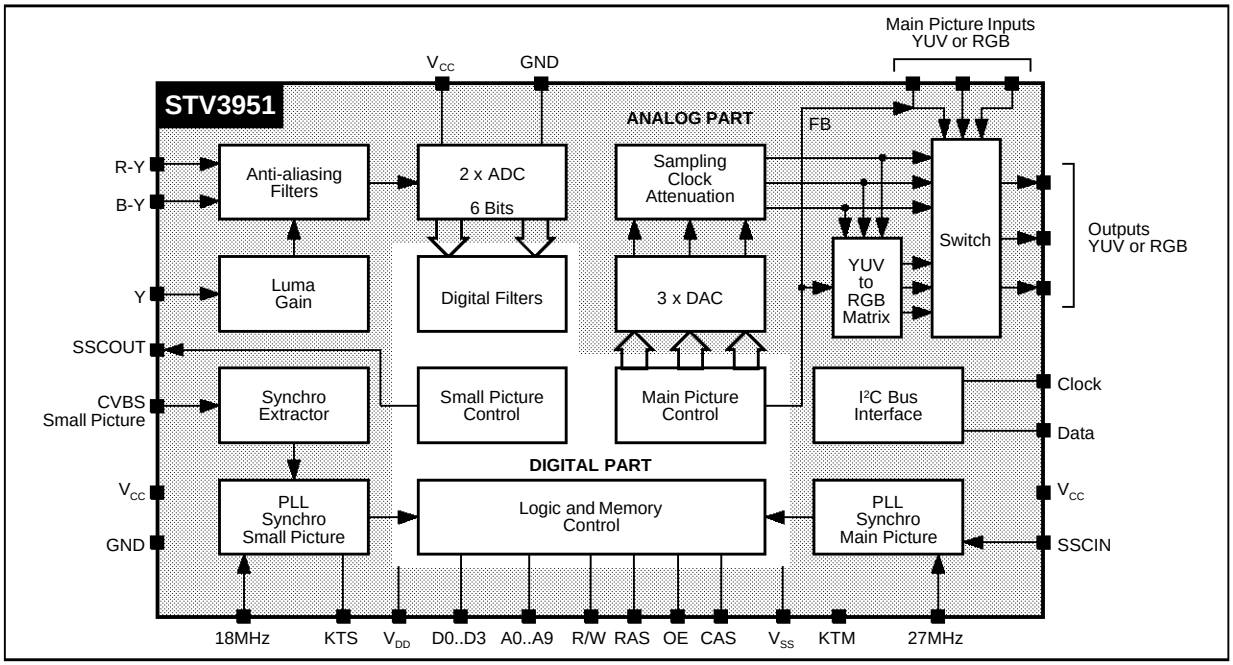
Pin No	Name	Description
1	VBOUT	V or B Output
2	UGOUT	U or G Output
3	YROUT	Y or R Output
4	YRM	Y or R Input of Main Picture, or FB Output (see Note)
5	UGM	U or G Input of Main Picture, or Not Connected (see Note)
6	VBM	V or B Input of Main Picture, or Not Connected (see Note)
7	SSCIN	Main Picture SSC Input
8	V_{CCM}	Main Picture Power Supply
9	LCM	Acquisition Clock Input (27MHz)
10	KTM	Time Constant for the Main Picture Line PLL
11	GND	Ground for Small and Main Pictures
12	KTS	Time Constant for the Small Picture Line PLL
13	LCS	Display Clock Input (18MHz)
14	V_{CCS}	Small Picture Power Supply
15	YS	Small Picture Y Input
16	US	Small Picture U Input
17	VS	Small Picture V Input
18	V_{ADC}	ADC Power Supply
19	GADC	ADC Ground
20	CVS	Small Picture Composite Synchronization Input
21	A8	Memory Address Bus Bit 8

Pin No	Name	Description
22	DGND	Digital Ground
23	A0	Memory Address Bus Bit 0
24	A1	Memory Address Bus Bit 1
25	A2	Memory Address Bus Bit 2
26	A3	Memory Address Bus Bit 3
27	A4	Memory Address Bus Bit 4
28	A5	Memory Address Bus Bit 5
29	A6	Memory Address Bus Bit 6
30	A7	Memory Address Bus Bit 7
31	OEnot	Output Enable (Inverted)
32	WEnot	Write Enable (Inverted)
33	CASnot	Column Address Enable (Inverted)
34	RASnot	Row Address Enable (Inverted)
35	SCL	I^2C Bus Clock Input
36	SDA	I^2C Bus Data Input
37	D3	Memory Data Bus Bit 3
38	D2	Memory Data Bus Bit 2
39	D1	Memory Data Bus Bit 1
40	D0	Memory Data Bus Bit 0
41	DV_{CC}	Digital Power Supply
42	SSCOUT	Small Picture SSC Output

3951-01.TBL

Note : In RGB mode with external insertion.

BLOCK DIAGRAM



3951-02.EPS

FUNCTIONAL DESCRIPTION

Display Possibilities

X and Y fine positions are programmable on all the screen area.
In case of several pictures, these are displayed vertically arranged and side by side.
1 small picture, moving or frozen, 1/4 or 1/3 reduction ratio (Figures 1 and 2).
2, 3 or 4 small pictures, with one moving or all frozen, according to 1/3 or 1/4 ratio (Figures 3 to 6).

Figure 1 : DRAM > 16K x 4

Figure 2 : DRAM > 64K x 4

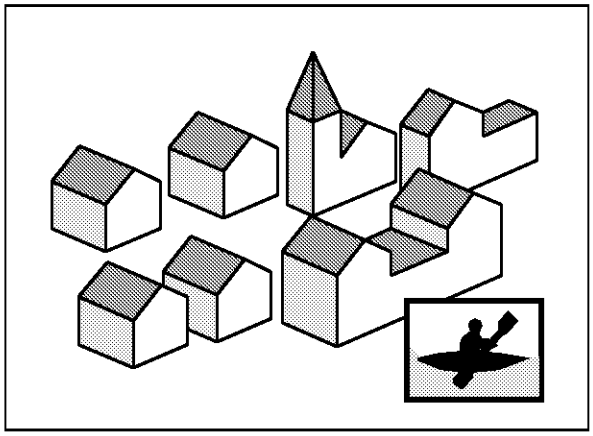


Figure 3 : DRAM > 64K x 4

Figure 4 : DRAM > 64K x 4

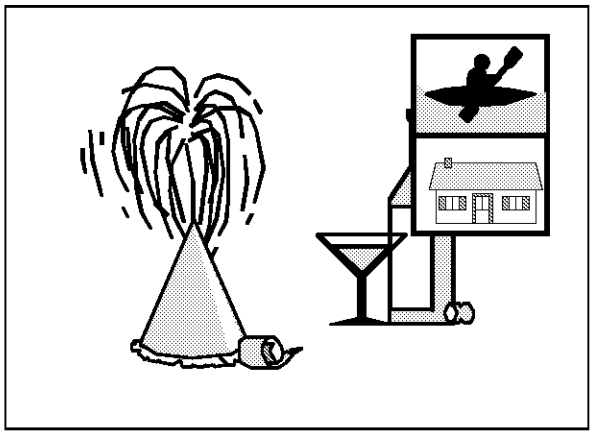


Figure 5 : DRAM > 64K x 4

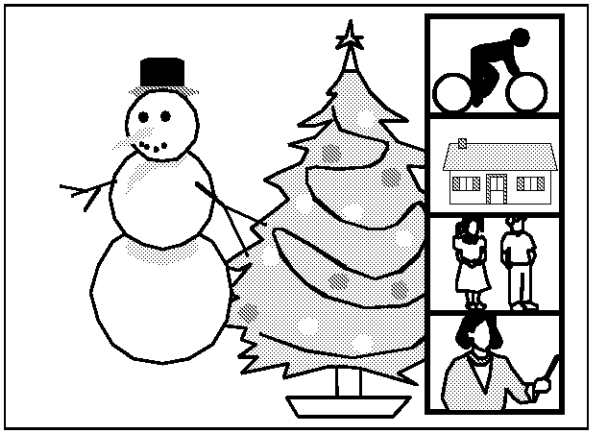
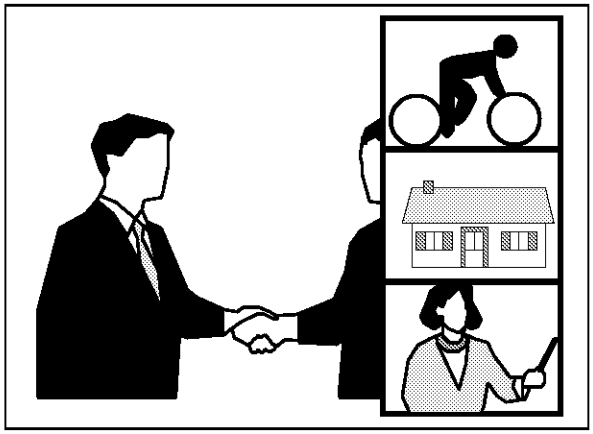


Figure 6 : DRAM > 256K x 4



FUNCTIONAL DESCRIPTION (continued)

Synchronization Possibilities

The STV3951 supports every combinations of 50/60Hz scanning and 50/60Hz source for the small picture (Neverveless, the frame dimensions is affected when 50 and 60Hz sources and display are mixed) (Examples Figures 7 and 8).

Figure 7 : 50Hz 625 Lines Scanning Mode

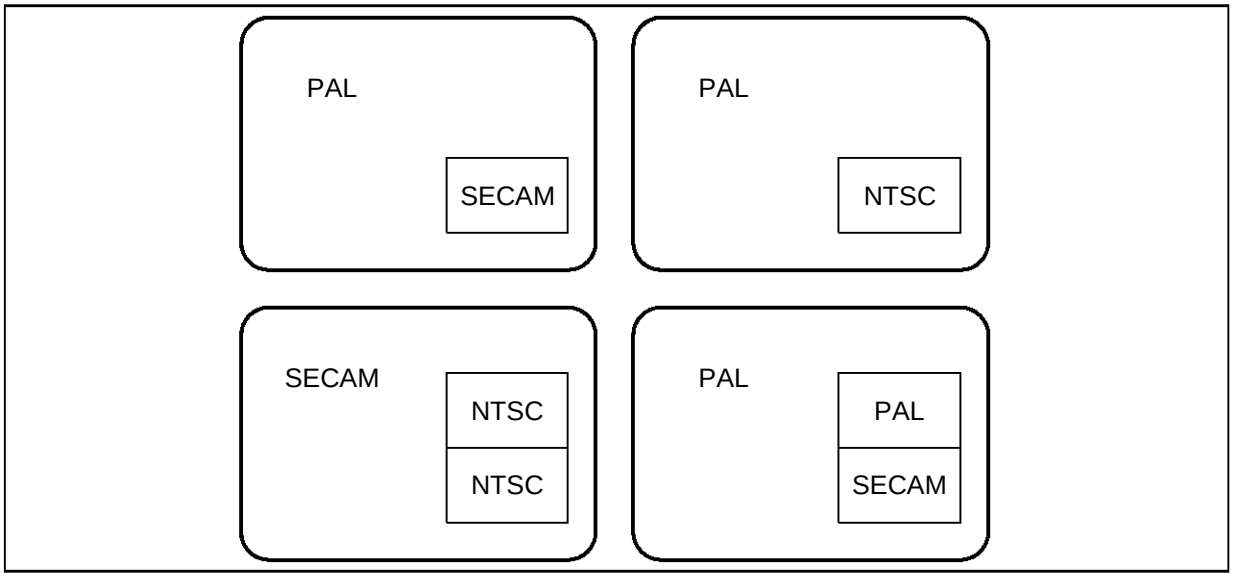
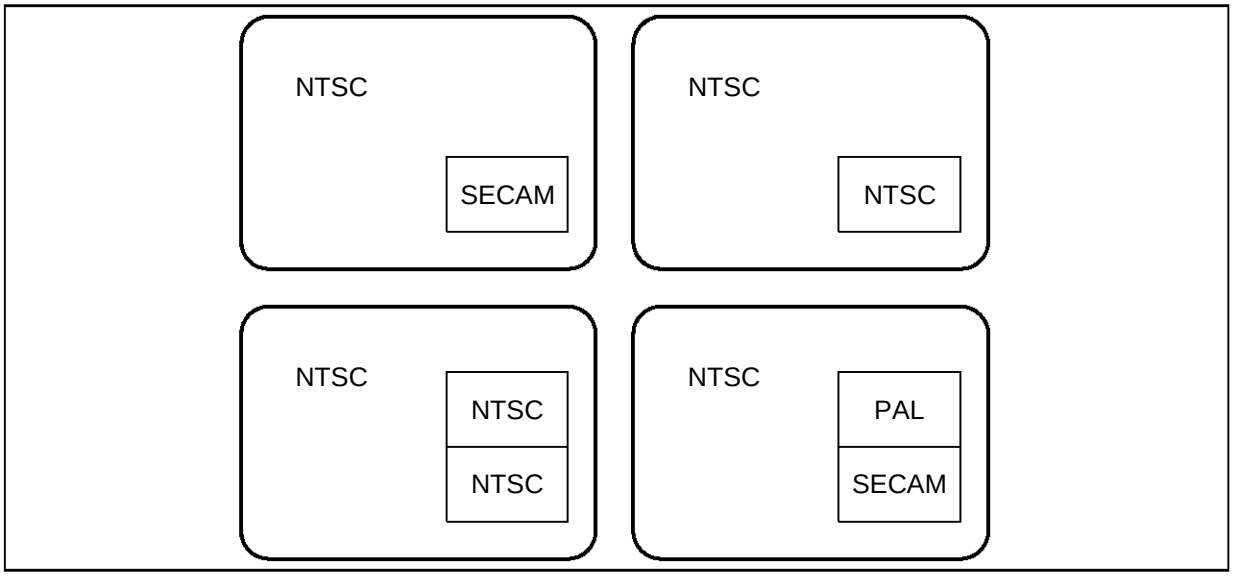


Figure 8 : 60Hz 525 Lines Scanning Mode



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage SDA, SCL, D3-D0	-0.3, 5.5	V
V_O	Ouput Voltage A8-A0, OE, WE, RAS, CAS	-0.3, 5.5	V
T_{stg}	Storage Temperature	-20, +125	°C
T_{oper}	Operating Ambient Temperature	0, +70	°C

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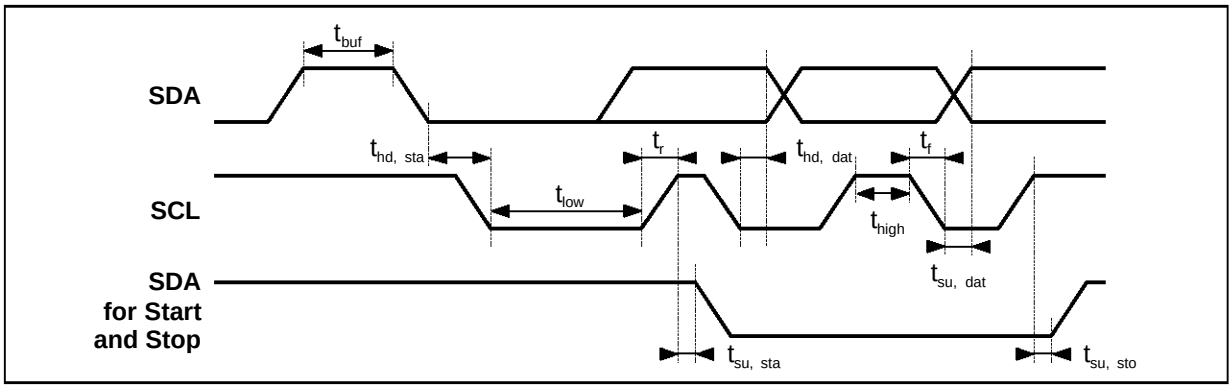
ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Digital Supply Voltage	4.5	5	5.5	V
I_{DD}	Digital Supply Current		2.5		mA
V_{CCM}	Analog Supply Voltage for Main Picture	8.1	9	9.9	V
I_{CCM}	Analog Supply Current (V_{CCM} = 9.9V)		25		mA
V_{CCS}	Analog Supply Voltage for Small Picture	8.1	9	9.9	V
I_{CCS}	Analog Supply Current (V_{CCS} = 9.9V)		30		mA
V_{ADC}	Analog Supply Voltage for A/D Conversion	8.1	9	9.9	V
I_{ADC}	Analog Supply Current (V_{ADC} = 9.9V)		15		mA
	Ratio between Analog 9V Supply : - Ratio V_{CCM}/V_{CCS} - Ratio V_{CCM}/V_{ADC}	 0.98 0.98		 1.02 1.02	
I^2C BUS INTERFACE					
SCL					
V_{IL}	Input Voltage Low Level	0		1	V
V_{IH}	Input Voltage High Level	3		V_{DD}	V
f_{SCL}	SCL Clock Frequency			400	kHz
t_r , t_f	Input Rise / Fall Times (10 to 90%)			2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 5.5V)			10	µA
C_I	Input Capacitance			7	pF
SDA					
V_{IL}	Input Voltage Low Level	0		1	V
V_{IH}	Input Voltage High Level	3		V_{DD}	V
t_r , t_f	Input Rise / Fall Times (10 to 90%)			2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 5.5V with Ouput Off)			10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0		0.5	V
t_{fo}	Output Fall Timebetween 3V and 1V			200	ns
C_L	Load Capacitance			400	pF
TIMING (see Figure 9)					
t_{LOW}	Low Period	4			µs
t_{HIGH}	High Period	4			µs
$t_{SU, DAT}$	Data Set-up Time	250			ns
$t_{HD, DAT}$	Data Hold Time	250			ns
$t_{SU, STO}$	Stop Set-up Time from Clock High	4			µs
t_{BUF}	Start Set-up Time following a Stop	4			µs
$t_{HD, STA}$	Start Hold Time	4			µs
$t_{SU, STA}$	Start Set-up Time following Clock Low to High Transition	4			µs

3951-03.TBL

Figure 9 : Serial Bus Timing



ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DIGITAL INPUT/OUTPUT					
D0-D3					
V_{IL}	Input Voltage Low Level	0		0.5	V
V_{IH}	Input Voltage High Level	2.3		V_{DD}	V
$I_{I(L)}$	Input Leakage Current (V_I = 5.5V and Ouput In high impedance state)			10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Output Voltage (I_{OL} = 1mA)	0		0.6	V
V_{OH}	High Output Voltage (I_{OH} = 0.2mA)	3		V_{DD}	V
t_r , t_f	Output Rise / Fall Time between 0.6V and 2.2V			50	ns
C_L	Load Capacitance			120	pF
$\overline{RAS}$, $\overline{CAS}$, A0-A8, $\overline{OE}$, $\overline{WE}$					
V_{OL}	Low Output Voltage (I_{OL} = 1mA)	0		0.6	V
V_{OH}	High Output Voltage (I_{OH} = 0.2mA)	3		V_{DD}	V
TIMING (see Figures 10 and 11)					
t_{rp}	RAS Precharge Time	90			ns
t_{cp}	CAS Precharge Time	40			ns
t_{asc}	Column Address Set-up Time	15			ns
t_{cah}	Column Address Hold Time	30			ns
t_{rah}	Row Address Hold Time	15			ns
t_{rcd}	RAS to CAS Delay Time	50			ns
t_{rsh}	RAS Hold Time	50			ns
t_{rac}	Access Time from RAS			120	ns
t_{cac}	Access Time from CAS			50	ns

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Figure 10 : Write Cycle

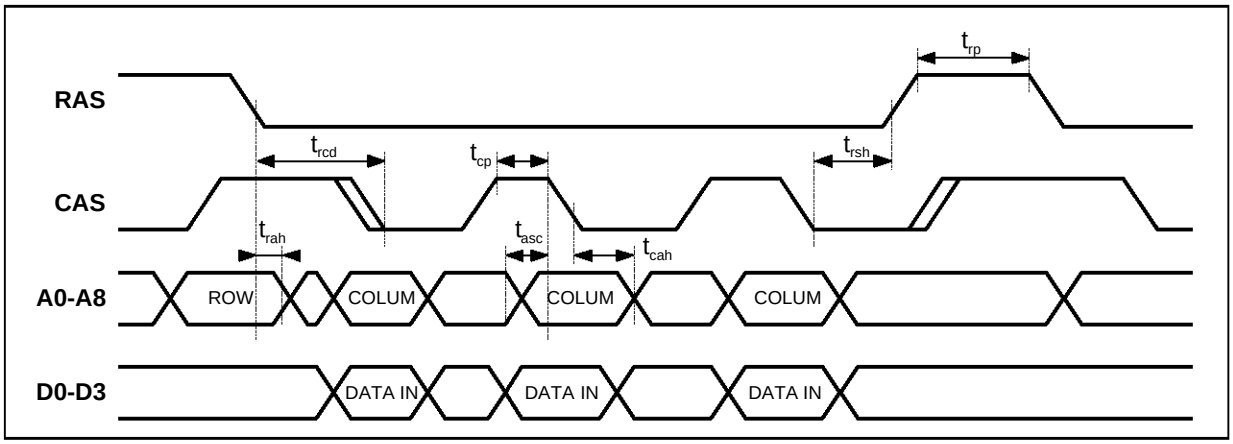
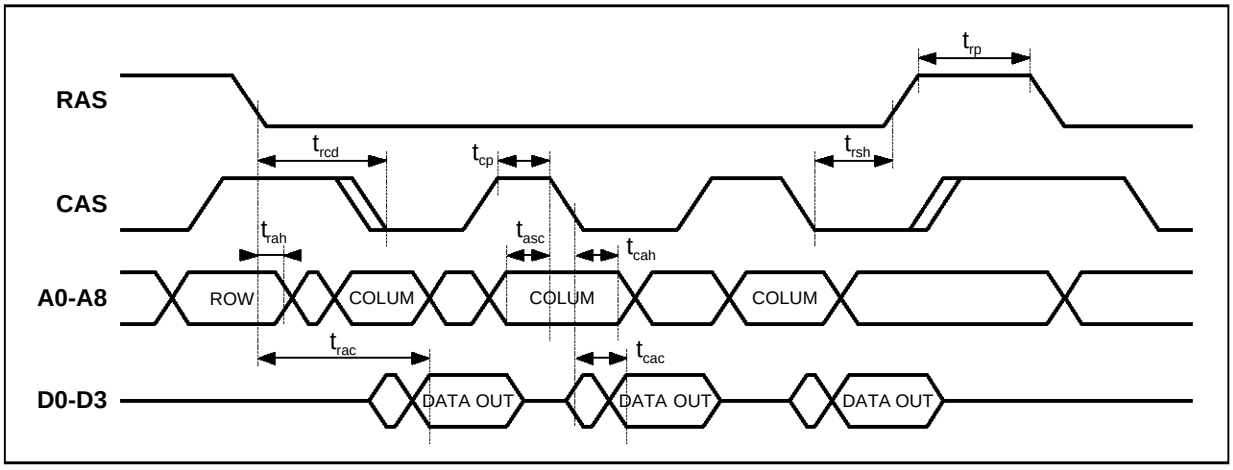


Figure 11 : Read Cycle



ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified)

Symbol	Pin	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SMALL PICTURE							
INPUTS							
V_{Samp}	17	Small Picture Input V(R-Y) Peak-to-peak Amplitude	See Figure 12			1.05	V
I_{cvs}		Clamp Current		±300		±500	µA
U_{Samp}	16	Small Picture Input U(B-Y) Peak-to-peak Amplitude	See Figure 13			1.27	V
I_{cus}		Clamp Current		±300		±500	µA
Y_{Samp}	15	Small Picture Y Black to White Amplitude	See Figure 14		0.7	1.4	V
I_{cys}		Clamp Current		±300		±500	µA
$G_{maxLuma}$ $G_{minLuma}$		Maximum Luminance Gain Minimum Luminance Gain	See Table 1		4.6 -3.1		dB dB
N_{gLuma}		Number of Gain Values			8		
SMALL PICTURE SYNCHRONIZATION							
CV_{Samp}	20	Top Synchro Amplitude with Nominal Width = 4.7µs	See Figure 15	30		600	mV
I_{push} I_{pull}		Up Current Down Current		250 35		450 65	µA µa
V_{okts}	12	Voltage Output Range for VCO Control of Small Picture	For V_{CCS} = 8.1V	2.3		7	V
V_{iaclcs}	13	Small Picture Clock (18MHz) Input Peak-to-peak Amplitude	DC offset = 2V, V_{DD} = 5V	0.5		V_{DD}-2	V
V_{idclcs}		Voltage DC	AC = 500mV, V_{DD} = 5V	1.5		V_{DD}-2	V
SSCOUT (Super Sand Castle Output) (see Figures 16 and 17)							
V_L	42	Low Level Voltage	I_m = 4.5mA			0.6	V
V_{FB}		Frame Blanking Level		2		3	V
V_{LB}		Line Blanking Level		4		5	V
V_{BG}		Burst Gate Level		7.2		V_{ADC}	V
I_m		I_{max}				4.5	mA

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ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified)

Symbol	Pin	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MAIN PICTURE							
INPUTS							
	UGM	Main Picture Input : U(B-Y) in Mode YUV (see Figure 13), G in Mode RGB (see Figure 18)					
V_{uamp} V_{gamp}	5	Peak-to-peak Amplitude			1.33 0.7	1.8 1.4	V V
IC_{ugm}		Clamp Current			±400		µA
	VBM	Main Picture Input : V(R-Y) in Mode YUV (see Figure 12), B in Mode RGB (see Figure 18)					
V_{vamp} V_{bamp}	6	Peak-to-peak Amplitude			1.05 0.7	1.4 1.4	V V
IC_{vbm}		Clamp Current			±400		µA
	YRM	This pin can be used as an input or as an output : - Mode YUV Channel Y (Input) (see Figure 14) - Mode RGB with Internal Insertion Channel R (Input) (see Figure 18) - Mode RGB with External Insertion (Output) : In this Mode, the Pin YRM outputs the Small Picture Insertion Signal (Named Fast Blanking) (see Figure 19)					
V_{yamp} V_{ramp}	4	Black to White Amplitude Peak-to-peak Amplitude			0.7 0.7	1.4 1.4	V V
IC_{yrm}		Clamp Current			±400		µA
V_{lofb}		Voltage during Main Picture Display (low impedance state)	V_{OUT} for I_{IN} = 2mA			300	mV
$V_{OUT(Max.)}$		Maximum Voltage				V_{DD}	V
I_{maxfb}		Current during Small Picture Insertion (high impedance state)	$I_{IN\ (Max.)}$ for V_{OUT} = 5V and R = 2.2kΩ			60	µA
MAIN PICTURE SYNCHRONIZATION							
V_{oktm}	10	Voltage Output Range for VCO Control (27MHz)	V_{CC} = 8.1V	2.3		7	V
V_{idclcm}	9	Display Clock DC Voltage (27MHz)	AC = 500mV, V_{DD} = 5V	1.5		V_{DD}-2	V
V_{iaclcm}		Display Clock Peak-to-peak Amplitude	DC offset = 2V, V_{DD} = 5V	0.5		V_{DD}-2	V
V_{iFB}	7	Frame Blanking Detection Level	See Figure 20	0.7		0.9	V
V_{iBG}		Burst Gate Detection Level	See Figure 20	3.0		3.5	V
V_{max}		Input Maximum Voltage				V_{DD}	V

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ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified)

Symbol	Pin	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUTS							
YUV MODE - OM1 = 0, OM2 = 0							
		UGOUT (see Figure 13)					
V_{unom} V_{umax}	2	Amplitude of Small Picture	Nominal contrast, nominal saturation and 1.27V on US Maximum contrast, maximum saturation and 1.27V on US		1.27 3.13		V
G_u		Gain of Main Picture between 0 and 6MHz			0		dB
V_{udc}		Black Level		3.6		5.0	V
		VBOUT (see Figure 12)					
V_{vnom} V_{vmax}	1	Amplitude of Small Picture	Nominal contrast, nominal saturation and 1.05 on VS Maximum contrast, maximum saturation and 1.05 on VS		1 2.5		V
G_v		Gain of Main Picture between 0 and 6MHz			0		dB
V_{vdc}		Black Level		3.6		5.0	V
		YROUT (see Figure 14)					
V_{ynom} V_{ymax}	3	Amplitude of Small Picture	Luminance gain : LG3 = 0, LG2 = 1, LG1 = 1 Nominal contrast and 0.7 on YS Maximum contrast and 0.7 on YS		 0.7 1.1		V
G_y		Gain of Main Picture between 0 and 6MHz			0		dB
V_{ydc}		Black Level		3.6		5.0	V
RGB MODE - OM1 = 1, OM2 = 0 OR OM1 = 0, OM2 = 1 (Y_{Samp} = 0.7V ; V_{Samp} = 0 ; U_{Samp} = 0 ; Luma gain : LG3 = 0, LG2 = 0, LG1 = 1)							
		UGOUT (see Figure 18)					
V_{gnom} V_{gmax}		Amplitude of Small Picture	Nominal contrast and nominal saturation Maximum contrast and maximum saturation		0.7 1.1		V V
G_g		Gain of Main Picture between 0 and 6MHz			0		dB
V_{gdc}		Black Level		3.3		4.7	V
		UBOUT (see Figure 18)					
V_{bnom} V_{bmax}		Amplitude of Small Picture	Nominal contrast and nominal saturation Maximum contrast and maximum saturation		0.7 1.1		V V
G_b		Gain of Main Picture between 0 and 6MHz			0		dB
V_{bdc}		Black Level		3.3		4.7	V
		YROUT (see Figure 18)					
V_{rnom} V_{rmax}		Amplitude of Small Picture	Nominal contrast and nominal saturation Maximum contrast and maximum saturation		0.7 1.1		V V
G_r		Gain of Main Picture between 0 and 6MHz			0		dB
V_{rdc}		Black Level		3.3		4.7	V
CONTRAST AND SATURATION GAIN OF THE SMALL PICTURE ON OUTPUTS							
$G_{maxcont}$ $G_{mincont}$	1 2-3	Maximum Contast Minimum Contast	Nominal saturation : SAT1 = 1, STA2 = 1, SAT3 = 0		4 -4.5		dB dB
G_{maxsat} G_{minsat}	2-3	Maximum Saturation Minimum Saturation	Nominal contast : CST1 = 1, CST2 = 1, CST3 = 0		4 -4.5		dB dB

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Figure 12

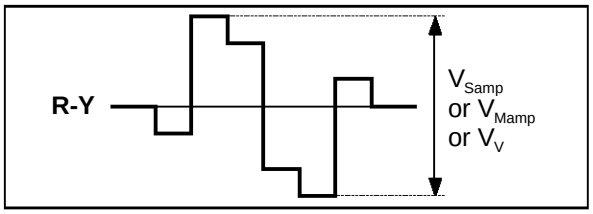


Figure 13

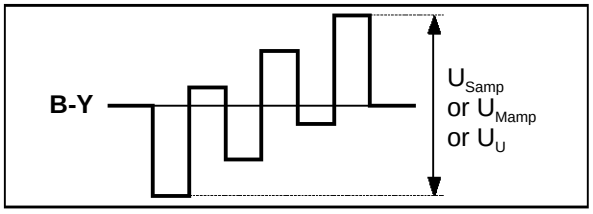


Figure 14

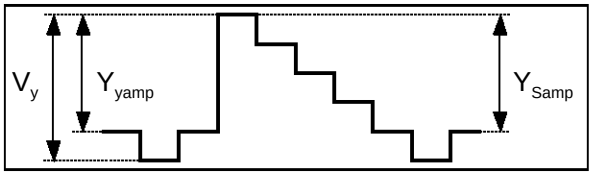


Figure 15

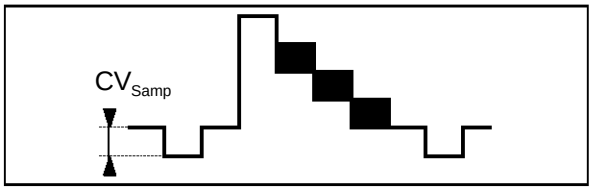


Figure 16

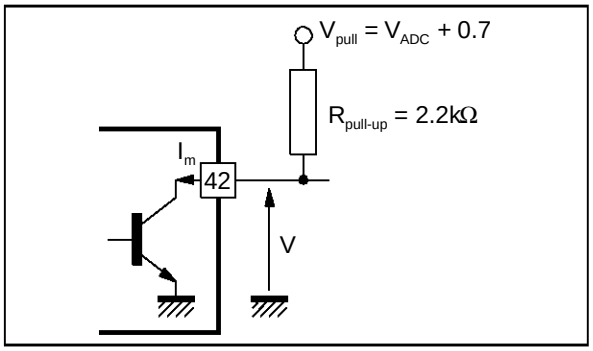


Figure 17

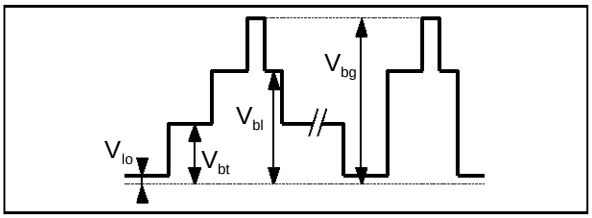


Figure 18

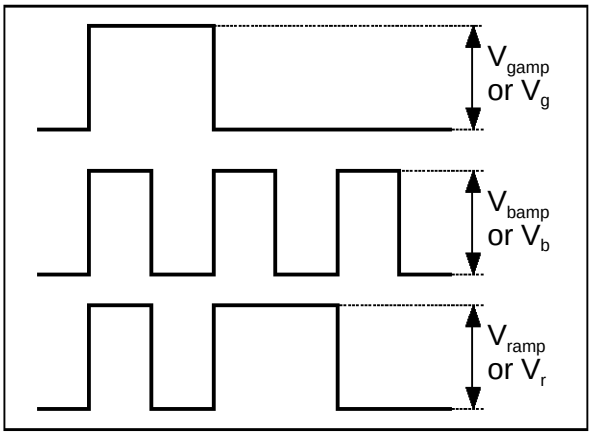


Figure 19

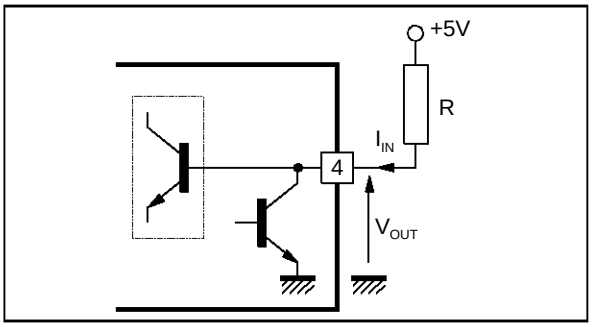
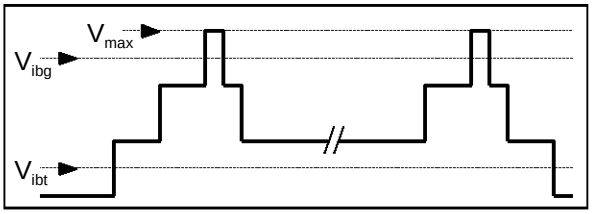


Figure 20



I²C BUS CONTROL

Slave Address

0010	111X
2	E

Address Mapping

Sub Address	Controls
0	Horizontal Position
1	Vertical Position
2	Border Colour + Luma Gain
3	Picture Control
4	Operating Mode
5	Saturation and Contrast
F	Reset after Power On

Sub Address 0 : Horizontal Position

MSB : 7
LSB : 0

The programmed value gives the left edge small picture position versus main picture start (see Figure 21).

Sub Address 1 : Vertical Position

MSB : 7
LSB : 0

Give the top edge small picture position per step of 2 lines : 256 steps maximum (see Figure 22).

Sub Address 2 : Border Colour + Luma Gain + Automatic Gain Control + Synchronisation

MSB							LSB
C3	C2	C1	AGC1	0	LG3	LG2	LG1

C3, C2, C1 : Border Colour

C3	C2	C1	
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

AGC1 : Automatic Gain Control

0 No automatic gain control.
1 Allow that luma gain been controlled by an automatic gain control.

LG3, LG2, LG4 : See Table 1

I²C BUS CONTROL (continued)

Table 1 (see Figure 23)

Input Signal Amplitude to be fixed to obtain V_{nbo} = 1V for Internal Processing		Logic Control			Gain (Typ.)	
V_{nbi}	V_{ppi}	LG3	LG2	LG1	Linear	dB
0.59	0.84	0	0	0	1.69	4.58
0.7	1	0	0	1	1.43	3.1
0.82	1.2	0	1	0	1.22	1.72
0.94	1.34	0	1	1	1.06	0.54
1.05	1.5	1	0	0	0.95	-0.42
1.18	1.68	1	0	1	0.84	-1.43
1.32	1.88	1	1	0	0.76	-2.41
1.44	2.05	1	1	1	0.69	-3.16

Figure 21

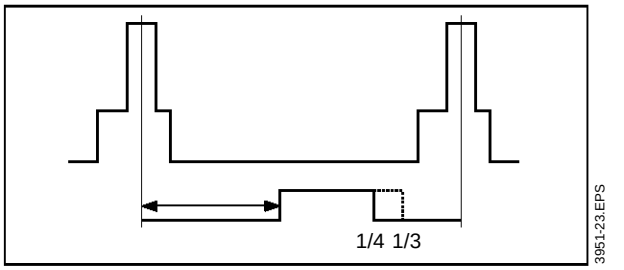


Figure 22

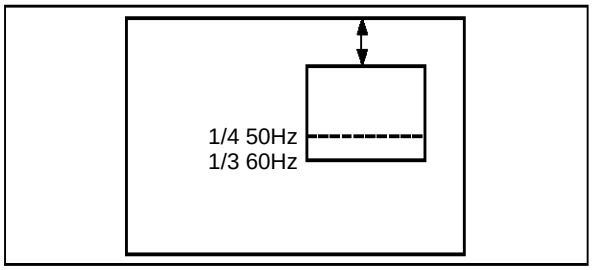
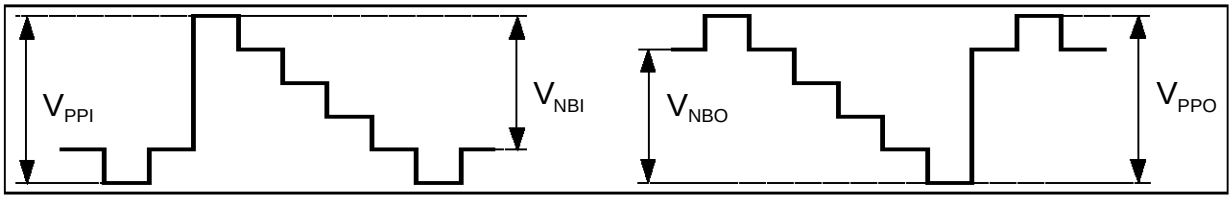


Figure 23 : Input and Output Signal



Sub Address 3 : Picture Control

MSB							LSB
0	D2	D1	E2	E1	FORMAT	PC1	PC0

D2, D1 : Number of the picture to be displayed.

D2	D1	
0	0	One picture displayed (Picture 1)
0	1	Two pictures displayed (Pictures 1 and 2)
1	0	Three pictures displayed (Pictures 1, 2 and 3)
1	1	Four pictures displayed (Pictures 1, 2, 3 and 4) (only 1/4 Format)

E2, E1 : Number of the picture to be edited (or loaded inside memory).

E2	E1	
0	0	Picture N1 moving
0	1	Picture N2 moving
1	0	Picture N3 moving
1	1	Picture N4 moving (only 1/4 Format)

FORMAT : 0 PIP Format 1/3
1 PIP Format 1/4

PC1, PC0 : On/Off Control (see Table 2)

Note : Only one picture moving at the same time.

I^2C BUS CONTROL (continued)

Table 2

Action	PC1	PC0	Edition	Display	Dram Refresh
No Memory Address	0	0	Off	Off	Off
No Picture	0	1	Off	Off	On
Still Picture	1	0	Off	On	On
Moving Picture	1	1	On	On	On

Sub Address 4 : Operation Mode

MSB							LSB
OM7	1	1	0	0	OM2	OM1	OM0

OM7 : 0 : Chroma "on"
1 : Chroma "off" (u, v = 0)

OM1, OM2 : Display mode (Small picture is always Y, U, V)

OM2	OM1		
0	0	Main : y, u, v	Out : y, u, v
0	1	Main : R, G, B	Out : R, G, B
1	0	Main : No	Out : R, G, B
1	1	Test Reserved	

OM0 : Chroma polarity inversion
0 : +U, +V
1 : -U, -V

Sub Address 5 : Saturation and Contrast and U/V Polarity and Bandwith Channel Y

MSB							LSB
BINV-U/V	BPY	CST3	CST2	CST1	SAT3	SAT2	SAT1

BPY : Allow to choose the bandwith of channel y
BPY : 0 → BW = 2MHz (1/3MHz)
BPY : 1 → BW = 1.5MHz (1/4MHz)

BINV_U/V : Allow to fonction with either +U and +V or -U or -V.
BINV_U/V : 0 → +U, +V
BINV_U/V : 1 → -U, -V

CST1, CST2, CST3 : Contrast control : 8 steps - Range : -4.5dB to +4dB (see note)

SAT1, SAT2, SAT3 : Saturation control : 8 steps - Range : -4.5dB to +4dB (see note)

Note : Saturation and contrast control concern all pictures displayed on the screen, at the same time.

Sub Address F : Power-on Reset

MSB							LSB
0	0	0	0	0	0	0	RESET

RESET : 1 Power on reset
0 Normal operation mode

Figure 24 : TV Typical Application

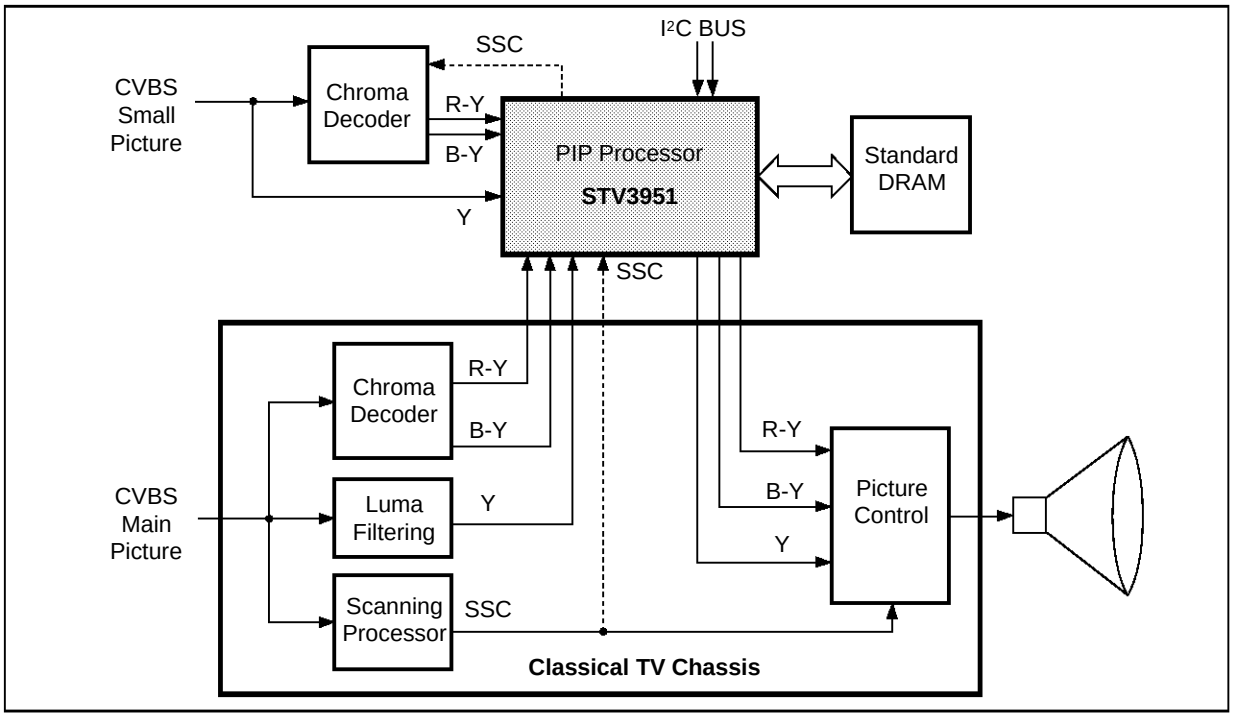


Figure 25 : External RGB Insertion

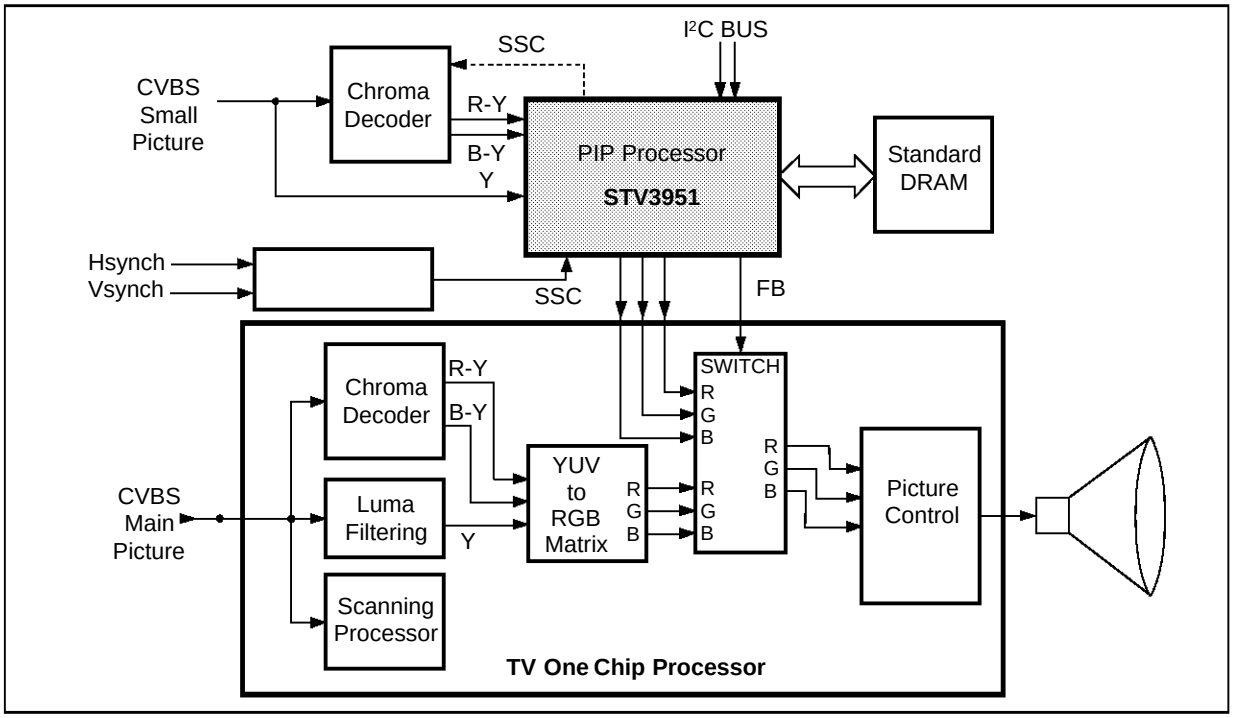


Figure 26 : Typical PIP Module for YUV Chassis

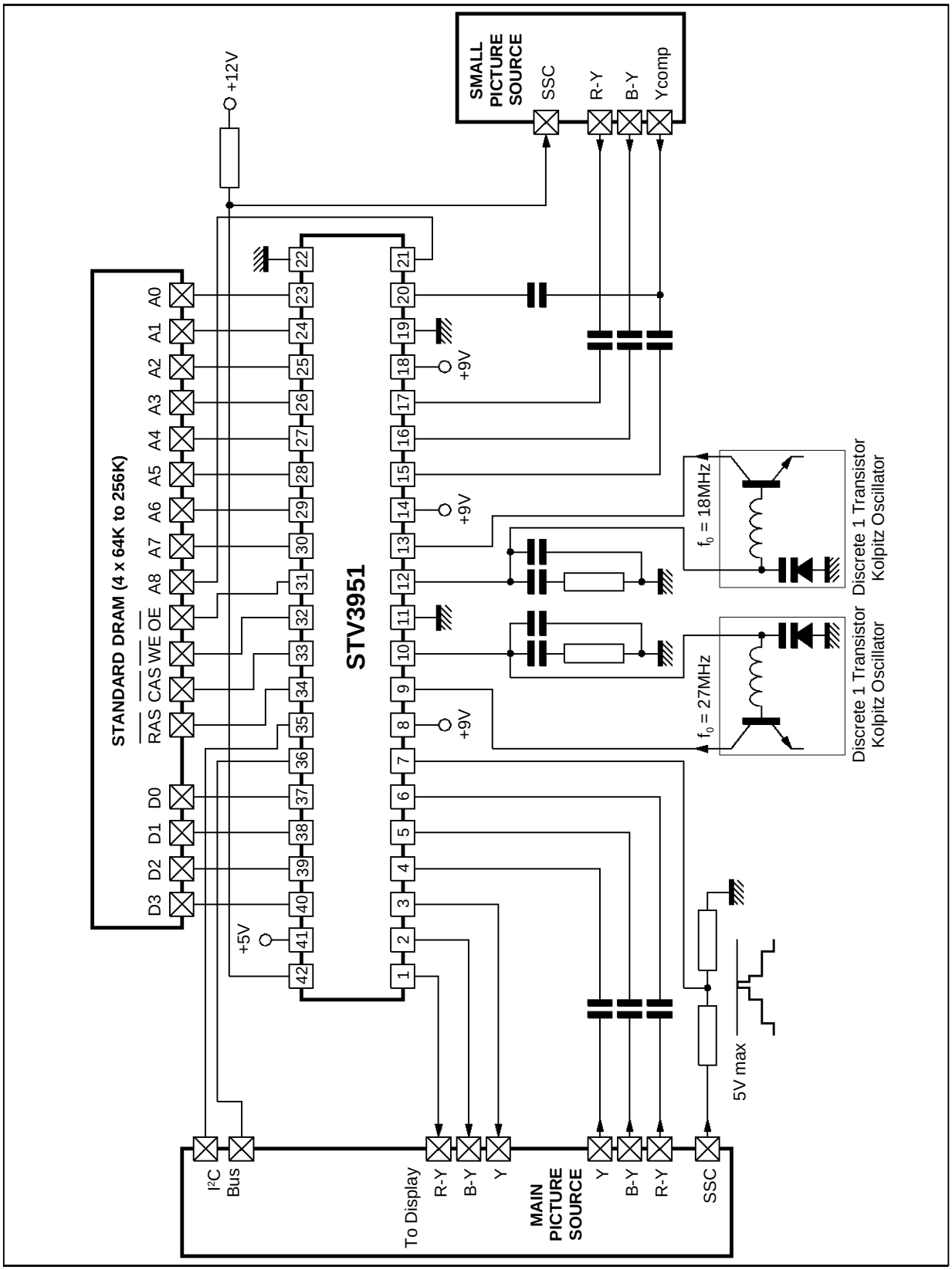
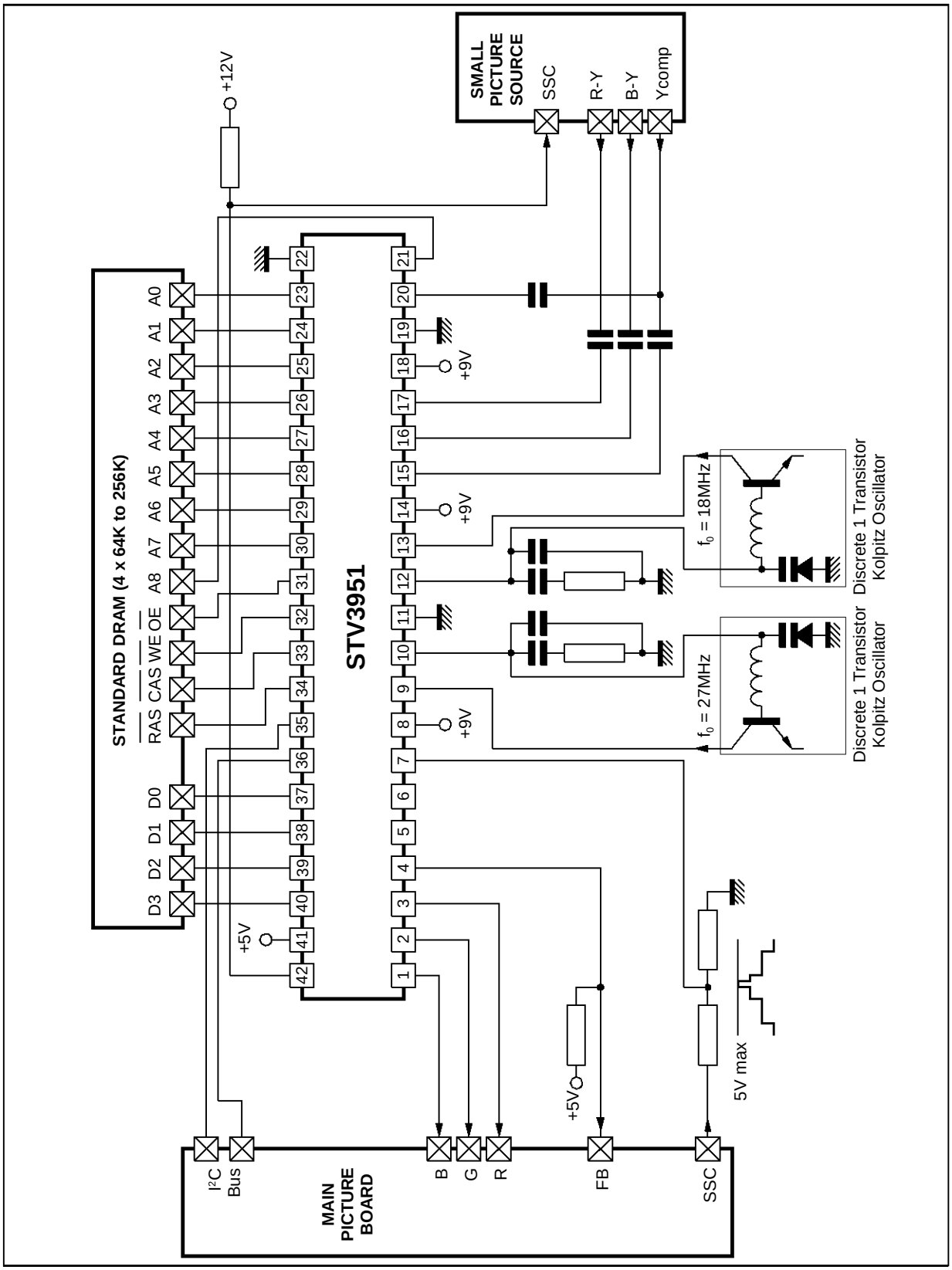
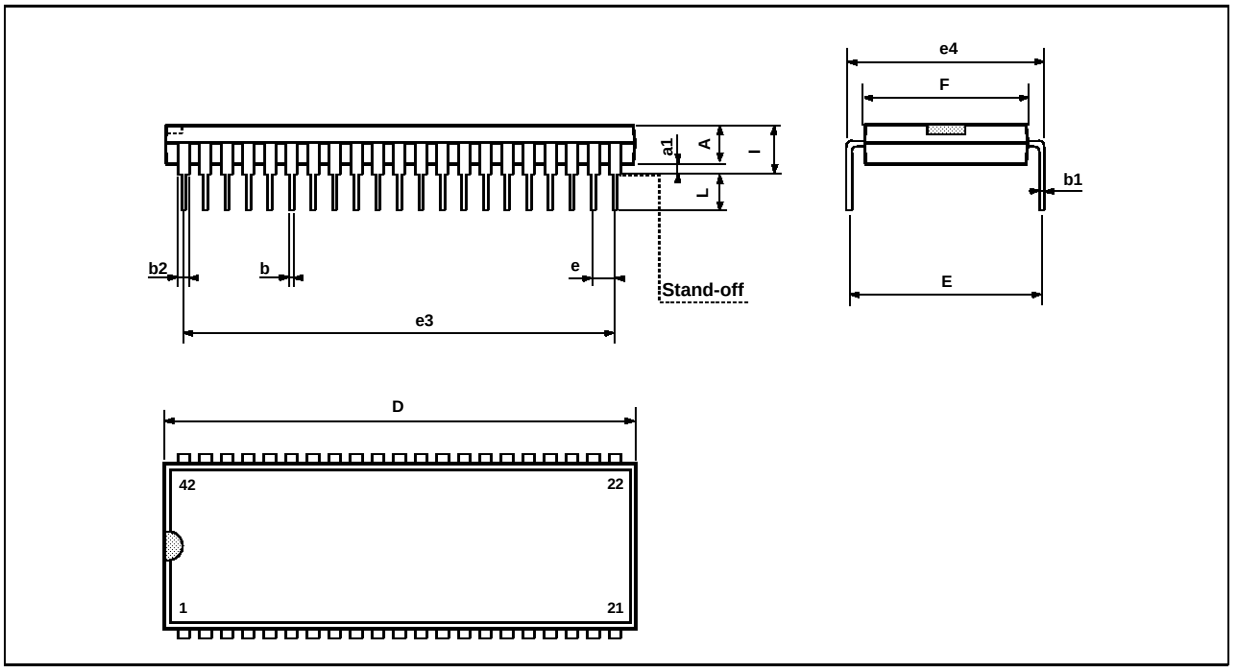


Figure 27 : Typical PIP Module for RGB Chassis



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.056
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
i			5.08			0.200
L		2.54			0.100	

SDIP42.TBL